Remarks

Reconsideration of this Application is respectfully requested.

Upon entry of the foregoing amendment, claims 1-2 and 4-22 are pending in the application, with 1 and 8 being the independent claims. Claim 1 is sought to be amended. Claims 7 and 23-24 are sought to be cancelled without prejudice to or disclaimer of the subject matter therein. These changes are believed to introduce no new matter, and their entry is respectfully requested.

Based on the above amendment and the following remarks, Applicants respectfully request that the Examiner reconsider all outstanding objections and rejections and that they be withdrawn.

Objection to the Claims

Claims 23 and 24 are objected to for various informalities. Claims 23-24 have been cancelled, thereby rendering the objection to those claims moot.

Rejections under 35 U.S.C. § 102

The Examiner has rejected claims 1-2, 5-8, and 23-24 under 35 U.S.C. § 102(e) as anticipated by U.S. Patent No. 6,704,863 to Paul *et al.* ("Paul"). Based on the foregoing amendments and for the reasons set forth below, Applicants respectfully traverse.

Independent claim 1, as presently amended, is directed to a method of processing an interrupt verification support mechanism in a computer system that includes a

processor and an input for external interrupts communicatively coupled to the processor. The method includes the steps of:

> (a) processing at least one actual instruction in the processor; and
>
> (b) if an external interrupt request or an interrupt pseudo-instruction is received by the processor, comparing data content of a program counter with data content of an interrupt register and replacing the actual instruction in an instruction fetch stage of the processor with the pseudo-instruction when the data content of the program counter matches the data content of the interrupt register, or when an external interrupt is present.

Paul does not teach or suggest each and every feature of independent claim 1 as presently amended. For example, as will be explained in more detail below, Paul does not teach or suggest "comparing data content of a program counter with data content of an interrupt register and replacing the actual instruction in an instruction fetch stage of the processor with the pseudo-instruction when the data content of the program counter matches the data content of the interrupt register" as recited by claim 1.

Paul is directed to a processor that provides reduced latency and loss of processor bandwidth when responding to an interrupt. Paul's processor achieves this, in part, by directly inserting the interrupt instructions into the pipeline of the processor. *See* Paul, col. 3, ll. 20-29. Interrupt handling circuitry, shown in FIG. 5 of Paul, detects the occurrence of an interrupt and than subsequently handles the interrupt by stalling the pipeline and inserting the interrupt instruction into a predetermined pipeline stage. *See* Paul, col. 8, ll. 34-44. In Paul, the stalled instruction is determined arbitrarily based on when the interrupt is received. When an interrupt occurs, it is simply processed by the interrupt handling circuitry and the associated instruction is inserted into the processor pipeline.

In contrast to the teachings of Paul, independent claim 1 recites "comparing data content of a program counter with data content of an interrupt register and replacing the actual instruction in an instruction fetch stage of the processor with the pseudo-instruction when the data content of the program counter matches the data content of the interrupt register." A specific implementation of this feature is shown in FIG. 4 and described at page 21, lines 16-18, of the specification of the present application, which states: "When the program counter PC matches the interrupt register, or an external interrupt is present, the actual instruction is replaced with a pseudo-instruction." The value stored in the interrupt register allows for the precise point at which an interrupt is to occur in a stream of instructions. Unlike Paul, in the event of an interrupt request, the interrupt verification support mechanism of the current Specification does not proceed to stall the processor pipeline and simply insert the interrupt. Rather, in claim 1, before an interrupt's pseudo-instruction is inserted in the instruction stream, the data content of a program counter is compared to the data content of an interrupt register. If their respective values match, than the pseudo-instruction subsequently replaces "the actual instruction in an instruction fetch stage of the processor," as recited in claim 1. This feature is not taught or suggested by Paul.

Since Paul does not teach or suggest each and every feature of independent claim 1, it cannot anticipate that claim. Dependent claims 2 and 5-7 are likewise not anticipated by Paul for the same reasons as independent claim 1 from which they depend, and further in view of their own respective features. Accordingly, Applicants respectfully request that the rejection of claims 1-2 and 5-7 under 35 U.S.C. § 102(e) be reconsidered and withdrawn.

Independent claim 8, recites "wherein the device includes a set of one or more interrupt registers each of which contains information, the information including at least a program counter of the instruction which is to be interrupted." As discussed above in reference to claim 1, Paul does not teach or suggest the use of an interrupt register that stores the "program counter of the instruction which is to be interrupted." In Paul, interrupt handling circuitry detects that an interrupt request occurs and subsequently stalls the pipeline. Once the pipeline is stalled, the interrupt instruction is inserted into a predetermined stage in the pipeline (e.g., decode stage). *See* Paul, col. 8, ll. 39-44. No where does Paul contemplate the use of an interrupt register that stores "a program counter of the instruction which is to be interrupted", as recited in claim 1. A specific implementation of this interrupt register is illustrated in FIG. 4 and described at page 21, lines 16-18, of the specification of the present application, which states: "When the program counter PC matches the interrupt register, or an external interrupt is present, the actual instruction is replaced with a pseudo-instruction." The value stored in the interrupt register allows for the precise point at which an interrupt is to occur in a stream of instructions.

Since Paul does not teach or suggest each and every feature of claim 8, it cannot anticipate that claim. Dependent claims 23-24 have been cancelled. Accordingly, Applicants respectfully request that the rejection of claims 8 and 23-24 under 35 U.S.C. § 102(e) be reconsidered and withdrawn.

Rejections under 35 U.S.C. § 103

Claims 4 and 20-22 were rejected under 35 U.S.C. §103(a) as being allegedly unpatentable over Paul in view of Sproul, III, U.S. Patent No. 4,498,136 ("Sproul"). Applicants respectfully traverse this rejection.

Claim 4 depends from claim 1 and claims 20-22 depend from claim 8. Sproul does not overcome all the deficiencies of Paul relative to independent claims 1 and 8 described above. For at least these reasons, and further in view of their own features, dependent claims 4 and 20-22 are patentable over the combination of Paul and Sproul. Reconsideration and withdrawal of the rejection are therefore respectfully requested.

Claims 9-11 and 13-19 were rejected under 35 U.S.C. §103(a) as being allegedly unpatentable over Paul in view of Case *et al.*, U.S. Patent No. 4,777,587 ("Case"). Applicants respectfully traverse this rejection.

Claim 9-11 and 13-19 depend from claim 8. Case does not overcome all the deficiencies of Paul relative to independent claim 8 described above. For at least these reasons, and further in view of their own features, dependent claims 9-11 and 13-19 are patentable over the combination of Paul and Case. Reconsideration and withdrawal of the rejection are therefore respectfully requested.

Conclusion

All of the stated grounds of objection and rejection have been properly traversed, accommodated, or rendered moot. Applicants therefore respectfully request that the Examiner reconsider all presently outstanding objections and rejections and that they be withdrawn. Applicants believe that a full and complete reply has been made to the

outstanding Office Action and, as such, the present application is in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

Prompt and favorable consideration of this Amendment and Reply is respectfully requested.

Respectfully submitted,

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